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Attorney Docket No. 95-553-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title of the Invention:

PROBE CARD ASSEMBLY AND KIT, AND METHODS OF USING SAME

Inventors: ELDRIDGE, et al.

Filing Date: 11/9/95

Serial Number: 08/554,902

SUPPLEMENTAL INFORMATION DISCLOSURE CITATION

(Substitute PTO-1449)

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION is being submitted **prior to an action on the merits.**

NO FEE IS REQUIRED.

Charge any shortfall to Dep. Acct. 12-1445.

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION (2) is being provided in addition to:

(1) INFORMATION DISCLOSURE CITATION, filed 4/4/96
(3) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
(4) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96

Although not required, TITLES for the patent references are provided herewith, as an aid to the examiner.

Copies of these references may be found in the file of commonly-owned, copending U.S. Patent Application No. 08/340,144 and, although NOT provided herewith, will be supplied upon request of the examiner.

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Although not required, TITLES for the patent references are provided herewith, as an aid to the examiner.

It would appear that the most relevant ones of the references cited herein are those having the term "probe" or "test" in their title. For example, the following (from the lists at page 3, et seq., below):

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METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES HAVING A COPPER HEAT CAPACITOR AND/OR COPPER HEAT SINK

4,034,468 Koopman; 7/77 29/628
METHOD FOR MAKING CONDUCTION-COOLED CIRCUIT PACKAGE

4,009,485 Koenig; 2/77 357/68
SEMICONDUCTOR PELLET ASSEMBLY MOUNTED ON CERAMIC SUBSTRATE

4,003,621 Lamp; 1/77 339/59 M
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3,984,166 Hutchison; 10/76 339/17 CF
SEMICONDUCTOR DEVICE PACKAGE HAVING LEAD FRAME STRUCTURE WITH INTEGRAL SPRING CONTACTS

3,982,320 Buchoff, et al.; 9/76 29/630 R
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3,940,786 Scheingold, et al.; 2/76 357/74
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3,939,559 Fendley, et al.; 2/76 29/628
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3,926,360 Moister, Jr.; 12/75 228/180
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3,921,285 Krall; 11/75 29/626
METHOD FOR JOINING MICROMINIATURE COMPONENTS TO A CARRYING STRUCTURE

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3,623,649 Keisling; 11/71 228/15
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3,517,438 Johnson, et al.; 6/70 29/627
METHOD OF PACKAGING A CIRCUIT MODULE AND JOINING SAME TO A CIRCUIT SUBSTRATE

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I, the undersigned, hereby certify that this correspondence is being deposited as first class mail, with sufficient postage, addressed to Commissioner of Patents and Trademarks, Washington, DC 20231, on the date set forth below.

For the Applicant,

Gerald E. Linden 30,282 4/4/96
(407) 382-7966 date

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Attorney Docket No. 95-553-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title of the Invention:

PROBE CARD ASSEMBLY AND KIT, AND METHODS OF USING SAME

Inventors: ELDRIDGE, et al.

Filing Date: 11/9/95

Serial Number: 08/554,902

SUPPLEMENTAL INFORMATION DISCLOSURE CITATION
(Substitute PTO-1449)

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION is being submitted **prior to an action on the merits.**

NO FEE IS REQUIRED.

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This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION (3) is being provided in addition to:

(1) INFORMATION DISCLOSURE CITATION, filed 4/4/96
(2) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
(4) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96

Although not required, TITLES for the patent references are provided herewith, as an aid to the examiner.

Copies of these references may be found in the file of commonly-owned, copending U.S. Patent Application No. 08/340,144 and, although NOT provided herewith, will be supplied upon request of the examiner.

It would appear that the most relevant ones of the references cited herein are those having the term "probe" or "test" in their title. For example, the following (from the list at pp. 3, et seq):

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MULTI-CHIP MODULE TESTING

5,128,612 Aton, et al.; 7/92 324/158
DISPOSABLE HIGH PERFORMANCE TEST HEAD

5,123,850 Elder, et al.; 6/92 439/67
NON-DESTRUCTIVE BURN-IN TEST SOCKET FOR INTEGRATED CIRCUIT DIE

5,007,576 Congleton, et al.; 4/91 228/103
TESTABLE RIBBON BONDING METHOD AND WEDGE BONDING TOOL FOR MICROCIRCUIT DEVICE FABRICATION

4,937,203 Eichelberger, et al.; 6/90 437/51
METHOD AND CONFIGURATION FOR TESTING ELECTRONIC CIRCUITS AND INTEGRATED CIRCUIT CHIPS USING A REMOVABLE OUTER LAYER

4,884,122 Eichelberger, et al.; 11/89 357/71
METHOD AND CONFIGURATION FOR TESTING ELECTRONIC CIRCUITS AND INTEGRATED CIRCUIT CHIPS USING A REMOVABLE OVERLAY LAYER

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INTEGRATED TEST AND ASSEMBLY DEVICE

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SEMICONDUCTOR CONNECTION COMPONENTS AND METHODS WITH RELEASABLE LEAD SUPPORT

For the Applicant,

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Attorney Docket No. 95-553-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title of the Invention:

PROBE CARD ASSEMBLY AND KIT, AND METHODS OF USING SAME

Inventors: ELDRIDGE, et al.

Filing Date: 11/9/95

Serial Number: 08/554,902

SUPPLEMENTAL INFORMATION DISCLOSURE CITATION
(Substitute PTO-1449)

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION is being submitted **prior to an action on the merits.**

NO FEE IS REQUIRED.

Charge any shortfall to Dep. Acct. 12-1445.

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(2) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
(3) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96

Although not required, TITLES for the patent references are provided herewith, as an aid to the examiner.

Generally, the references presented herein are arranged in groups, as follows:

GROUP 1. References related to solder balls or solder pads as terminals of a semiconductor package or chip carrier. These references have particular pertinence to this application (08/584,981), and may be found in the file thereof.

COPIES OF THESE REFERENCES ARE **NOT** ENCLOSED HEREWITH, but will be provided upon request.

GROUP 2. References related to probing and/or testing semiconductor devices. These references have particular pertinence to this application and to commonly-owned, copending U. S. Patent Application No. **08/558,332.**

COPIES OF THESE REFERENCES ARE ENCLOSED HEREWITH.

GROUP 3. References related to previously-cited patent references and miscellaneous references of interest.

COPIES OF THESE REFERENCES ARE **NOT** ENCLOSED HEREWITH, AND MAY BE FOUND IN THE FILE OF commonly-owned, copending U.S. Patent Application No. 08/340,144. Copies of these references will be provided upon request.

GROUP 4. References cited in PCT/US94/13373

COPIES OF THESE REFERENCES ARE **NOT** ENCLOSED HEREWITH, AND MAY BE FOUND IN THE FILE OF commonly-owned, copending U.S. Patent Application No. 08/340,144. Copies of these references will be provided upon request.

GROUP 5 References dealing with making connections to electronic components.

COPIES OF THESE REFERENCES ARE **NOT** ENCLOSED HEREWITH, AND MAY BE FOUND IN THE FILE OF commonly-owned, copending U.S. Patent Application No. 08/340,144. Copies of these references will be provided upon request.

GROUP 1

U.S. Patent References:

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LEAD FRAME AND CHIP CARRIER HOUSING

GROUP 2

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